1938

April 2025

Time – Three hours
(Maximum Marks: 100)

[*N.B.* 1. Answer all questions under Part-A. Each question carries 3 marks.
2. Answer all the questions either (a) or (b) in Part-B. Each question carries 14 marks.]

PART – A

1. Implement NOT gate using NMOS.
2. What are the levels of abstractions in VLSI design?
3. Write a note on HDL.
4. Write the syntax for variable declaration.
5. State the functions of comparator.
6. Write a VHDL program for half adder.
7. What is flip flop? Mention its types.
8. Write a VHDL program for D flip flop.
9. Define FPGA.
10. Write about the design flow of ASIC.

[Turn over.....

PART – B

11. (a) Implement AND, OR, NAND and NOR using CMOS.

(Or)

(b) Explain the various steps involved in the VLSI design process.

12. (a) (i) Write the general format of VHDL program.(7)
(ii) Explain "if else" statement in VHDL with an example.(7)

(Or)

(b) Write a VHDL program for NOT, AND, OR, NAND, NOR and XOR gates.

13. (a) Describe the operation of four bit arithmetic adder.

(Or)

(b) Write a VHDL program for 4 to 1 multiplexer and 1 to 4 demultiplexer.

14. (a) Discuss the construction and working of 3 bit up/down counter.

(Or)

(b) Write a VHDL program for JK flip flop with reset input.

15. (a) Explain the architecture of CPLD with necessary diagrams.

(Or)

(b) Write short notes on PROM, PLA and PAL.
